WE CLAIM:

1. A method of creating a model of a data processing apparatus having a subsystem circuit under test and one or more surrounding circuits operable to provide input signals to and receive output signals from said subsystem circuit, said method comprising the steps of:

conducting a simulation of said data processing apparatus performing a test sequence of data processing operations including simulating operation of both said subsystem under test and said one or more surrounding circuits using a subsystem circuit model and a model of said one or more surrounding circuits;

recording input signals to and output signals from said subsystem circuit whilst performing said test sequence of data processing operations; and

using at least a representation of said recorded input signals to form a reduced model to replay said recorded input signals to said subsystem circuit model without requiring a periodic sampling reference and apply a plurality of sampling rules to output signals of said subsystem circuit model to sample said output signals and to compare said output signals with one or more predetermined characteristics indicative of correct operation;

whereby said subsystem model and said reduced model may be used to simulate said subsystem performing said test sequence of data processing operations without simulating operation of said one or more surrounding circuits.

2. A method as claimed in claim 1, wherein formation of said reduced model uses one or more configuration files including data specifying input signals to said subsystem circuit, output signals from said subsystem circuit and bi-directional signals exchanged with said subsystem circuit.

3. A method as claimed in claim 2, wherein signals from said subsystem are used to determine when bi-directional signals can be driven making allowance for variations in delays inherent in output loads.

4. A method as claimed in claim 1, wherein said reduced model includes a rule having an output signal time window within which a change in said output signal to a predetermined output signal value should occur to be indicative of correct operation.

5. A method as claimed in claim 4, wherein said predetermined output signal value is one of: high; low; changed; and high impedance.

6. A method as claimed in claim 1, wherein within said data processing apparatus at least one of said output signals is a strobe output signal used to trigger sampling of at least one strobed output signal, said reduced model including a rule whereby a change in said strobe output signal is detected and used to verify the correct state of the output signal.

7. A method as claimed in claim 6, wherein said rule includes a strobe output signal time window within which a change in said strobe output signal to a predetermined strobe output signal value should occur to be indicative of correct operation.

8. A method as claimed in claim 6, wherein said rule includes a strobed output signal time window within which said strobed output signal should hold a predetermined strobed output signal value to be indicative of correct operation.

9. A method as claimed in claim 8, wherein said strobed output signal time window is non-symmetrically disposed about a time when said strobed output signal is sampled.

10. A method as claimed in claim 8, wherein said strobed output signal time window is at least partially surrounded by a settling time window within which said strobed output signal is permitted to change.

11. A method as claimed in claim 10, wherein said settling time window is at least partially surrounded by a settled time window within which said strobed output signal is not permitted to change.

12. A method as claimed in claim 1, wherein said full subsystem circuit model from which said input signals and said output signals are recorded may be different

from that to which said input signals are subsequently replayed and from which output signals are subsequently analysed.

13. A method as claimed in claim 12, wherein said full subsystem circuit model may change between different versions during regression testing.

14. A method as claimed in claim 12, wherein said full subsystem circuit model may change between being one of an RTL model, a netlist model or other software view.

15. A method as claimed in claim 1, wherein changes in at least one of said output signals other than at sampling points for that output signal are also monitored.

16. A method as claimed in claim 1, comprising recording progress messages for replay during regression testing.

17. Apparatus for creating a model of a data processing apparatus having a subsystem circuit under test and one or more surrounding circuits operable to provide input signals to and receive output signals from said subsystem circuit, said apparatus comprising:

logic operable to conduct a simulation of said data processing apparatus performing a test sequence of data processing operations including simulating operation of both said subsystem under test and said one or more surrounding circuits using a subsystem circuit model and a model of said one or more surrounding circuits;

logic operable to record input signals to and output signals from said subsystem circuit whilst performing said test sequence of data processing operations; and

logic using at least a representation of said recorded input signals and one or more configuration files to form a reduced model to replay said recorded input signals to said subsystem circuit model and apply a plurality of sampling rules to output signals of said subsystem circuit model to sample said output signals and to compare said output signals with one or more predetermined characteristics indicative of correct operation;

whereby said subsystem model and said reduced model may be used to simulate said subsystem performing said test sequence of data processing operations without simulating operation of said one or more surrounding circuits.

18. A computer program product comprising a computer program for controlling a computer to perform a method as claimed in any one of claims 1 to 16.

19. A method of modelling a data processing apparatus having a subsystem circuit under test and one or more surrounding circuits operable to provide input signals to and receive output signals from said subsystem circuit, said method comprising the steps of:

providing a subsystem circuit model and a reduced model;

using said reduced model to apply a sequence of previously recorded input signals to a model of said subsystem circuit, said input signals corresponding to those provided by said one or more surrounding circuits to said subsystem circuit when performing a test sequence of data processing operations; and

using said reduced model to apply a sampling rule associated with each output signal of said subsystem circuit to sample said output signal and compare said output signal with one or more predetermined characteristics indicative of correct operation.

20. A method as claimed in claim 19, wherein said reduced model includes a rule having an output signal time window within which a change in said output signal to a predetermined output signal value should occur to be indicative of correct operation.

21. A method as claimed in claim 20, wherein said predetermined output signal value is one of:

high;

low;

changed; and

high impedance.

22. A method as claimed in claim 19, wherein within said data processing apparatus at least one of said output signals is a strobe output signal used to trigger sampling of at least one strobed output signal, said reduced model including a rule

whereby a change in said strobe output signal is detected and used to trigger sampling within said reduced model of said at least one strobed output signal.

23. A method as claimed in claim 22, wherein said rule includes a strobe output signal time window within which a change in said strobe output signal to a predetermined strobe output signal value should occur to be indicative of correct operation.

24. A method as claimed in claim 22, wherein said rule includes a strobed output signal time window within which said strobed output signal should hold a predetermined strobed output signal value to be indicative of correct operation.

25. A method as claimed in claim 24, wherein said strobed output signal time window is non-symmetrically disposed about a time when said strobed output signal is sampled.

26. A method as claimed in claim 24, wherein said strobed output signal time window is at least partially surrounded by a settling time window within which said strobed output signal is permitted to change.

27. A method as claimed in claim 26, wherein said settling time window is at least partially surrounded by a settled time window within which said strobed output signal is not permitted to change.

28. A method as claimed in claim 19, wherein said full subsystem circuit model from which said input signals and said output signals are recorded may be different from that to which said input signals are subsequently replayed and from which output signals are subsequently analysed.

29. A method as claimed in claim 28, wherein said full subsystem circuit model may change between different versions during regression testing.

30. A method as claimed in claim 28, wherein said full subsystem circuit model may change between being one of an RTL model, a netlist model or other software view.

31. A method as claimed in claim 19, wherein changes in at least one of said output signals other than at sampling points for that output signal are also monitored.

32. Apparatus for modelling a data processing apparatus having a subsystem circuit under test and one or more surrounding circuits operable to provide input signals to and receive output signals from said subsystem circuit, said apparatus comprising:

logic providing a subsystem circuit model and a reduced model;

logic using said reduced model to apply a sequence of previously recorded input signals to a model of said subsystem circuit, said input signals corresponding to those provided by said one or more surrounding circuits to said subsystem circuit when performing a test sequence of data processing operations; and

logic using said reduced model to apply a sampling rule associated with each output signal of said subsystem circuit to sample said output signal and compare said output signal with one or more predetermined characteristics indicative of correct operation.

33. A computer program product comprising a computer program for controlling a computer to perform a method as claimed in any one of claims 19 to 31.

34. A reduced hardware model synthesised from said reduced model of claim 1.